

● PRINTER RUSH ●

(PTO ASSISTANCE)

Application : <u>10/1083708</u>	Examiner : <u>Lam</u>	GAU : <u>2827</u>
From : <u>T. McGill</u>	Location : <u>IDC</u> FMF FDC	Date : <u>4-22-05</u>
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DOC CODE	DOC DATE	MISCELLANEOUS
<input type="checkbox"/> 1449	_____	<input type="checkbox"/> Continuing Data
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<input checked="" type="checkbox"/> SPEC	<u>10-10-03</u>	

[RUSH] MESSAGE: Specification page 2 line 3 has
a blank line. Please provide
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Thank You

[XRUSH] RESPONSE: corrected

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INITIALS: RP

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 REV 10/04

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Fig. 05

illustrative example of the reference voltage is a pre-charge voltage used, in operation, to bias bit lines and complement bit line bars of the DRAM device. ~~Variations of the reference voltage may reach about - % of a nominal value of the voltage.~~ Instability of the reference voltage causes asymmetry in detection of rising and falling edges of the digitized data and control signals, as well as random elongation or truncation of the signals, and, as such, may degrade signal-to-noise ratio and operational performance of the DRAM device.

[0004] Therefore, there is a need in the art for an improved method and circuit configuration for digitizing data and control signals in an input buffer of a DRAM device.

SUMMARY OF THE INVENTION

[0005] A method of digitizing data and control signals in an input buffer of a dynamic random access memory (DRAM) device. The method comprises supplying a plurality of buffer modules, each buffer module including a differential amplifier having a first input and a second input, a common source stage, and an output stage, supplying a source of a bias voltage and a source of a reference voltage, coupling the first input to a source of a data or control signal and coupling the second input to a source of a reference voltage, applying the bias voltage to control impedance of the common source stage, and applying the reference voltage to define the amplitude of the bias voltage.

[0006] Another aspect of the invention is a circuit configuration of an input buffer of data or control signals in a DRAM device. The input buffer comprises a plurality of buffer modules, wherein each buffer module includes a differential amplifier having a first input responsive to the signal and a second input responsive to a reference voltage, a common source stage, and an output stage, and a source of a bias voltage. The bias voltage controls impedance of the common source stage, while the amplitude of the bias voltage is defined by the reference voltage.